DRAWING AMENDMENTS

The attached drawing sheet includes changes to FIG. 1. This sheet, which only includes FIGs. 1, replaces the original sheet including FIG. 1. The "X" mark and the check mark in the circles of the legacy mode runtime have been revised to correspond to the text of the background section in paragraph [0006]. The mistake was inadvertent.

Attachment: Replacement Sheet

REMARKS

Claims 1-28 remain pending in the instant application. All claims presently stand rejected. Reconsideration of the pending claims is respectfully requested.

Specification

Paragraphs [0036] and [0039] of the Specification have been amended to cure inadvertent typographical errors.

Drawings

Prior art FIG. 1 has been amended to cure an inadvertent error. The amended FIG. 1, submitted herewith, is fully supported in paragraph [0006] of the Background Section. In particular, the "X" mark and the check marks were mistakenly placed in the wrong circles in the legacy mode runtime under the dashed line.

Claim Rejections – 35 U.S.C. § 112

Claims 1-28 stand rejected under 35 USC § 112, second paragraph, for omitting essential elements and for being indefinite.

Firstly, Applicants note that the Specification and the claims specifically discuss and recite "hardware interrupts"-- not software interrupts. Applicants note that it is important to read the Specification with this in mind.

Secondly, in section 6 of the Office Action, the Examiner asks, "What is generating the IRQ and how?" and "how is the processor in native mode (i.e., 32-bit or 64-bit execution mode) when it is executing 16-bit code?"

To answer the Examiner's question "what is generating the IRQ and how?", Applicants point the Examiner to FIG. 3 and related text. In the embodiment illustrated in FIG. 3, hardware entities of processing system 300 issue hardware IRQs (either legacy or native type) to interrupt controller 335, which then relays these hardware interrupts to processor 305. As discussed in the specification, an example device that may issue a hardware interrupt is an adaptor card 560 (see FIG. 5). The specification describes that adaptor card 560 may include a corresponding option ROM (corresponding to option ROMs 320 or 325 in FIG. 3). If adaptor card 560 is a legacy type device, then its option

ROM will include a legacy type interrupt service routine ("ISR") which is executed by processor 305 while operating in legacy mode runtime (see FIG. 2). If adaptor card 560 is a native type device, then its option ROM will include a native type ISR, which is executed by processor 305 while operating in native mode runtime (see FIG. 2).

Regarding the Examiner's second question. Neither the specification nor the claims state or recite that 16-bit code is executed while the processor is in native mode operation. Rather (this is discussed in more detail below) claim 1 recites, "receiving" a legacy type **hardware** IRQ during the native mode runtime and then servicing it. However, claim 1 does not state that the legacy type IRQ is serviced during the native mode runtime. The Examiner will note that claim 2 recites, transistioning to the legacy mode runtime to service the legacy type hardware IRQ.

Thirdly, in section 7 of the Office Action, the Examiner notes that the embodiment disclosed includes a global interrupt handler that executes in native mode runtime, and then asks, "[i]f that is true then it would seem legacy type hardware interrupts could not reasonably be defined 'as hardware IRQ that is serviced with 16-bit code', since it seems to require both 16-bit and 32-bit code to service it."

The Specification clearly states that a legacy type IRQ is "serviced" while processor 305 is operating in the legacy mode runtime (see FIG. 2); however, this does not mean that a legacy type IRQ cannot be "received" during the native mode runtime. As illustrated in FIG. 2, legacy type hardware IRQ 205 is received while operating in the native mode runtime. While prior art methods would mask this interrupt event off (and therefore not even receive it) until such time as the processor synchronously transitions to the legacy mode runtime or even just ignore it, embodiments of the invention will transition to the legacy mode runtime specifically in response to receiving the legacy type IRQ while operating in the native mode runtime. In one embodiment, this is accomplished via global interrupt handler 379. The global interrupt handler 379 will call down to the corresponding legacy type ISR, at this point processor 305 will transition to the legacy mode runtime, and the legacy type ISR will "service" the legacy type hardware IRQ.

It is important to note that claim 1 recites, receiving a legacy type IRQ during a native mode runtime and then servicing that legacy type hardware IRQ that was received

during the native mode runtime. It does not state that the legacy type IRQ is serviced "during" the native mode runtime. In fact, claim 2 specifically recites "transitioning from the native mode runtime to the legacy mode runtime in response to the legacy type hardware IRQ..." Element 2 of claim 1 states that the legacy type hardware IRQ is serviced, it does not state that it is serviced during the native mode runtime, rather it simply states that the legacy type hardware IRQ was received during the native mode runtime. Applicants respectfully submit that the disclosure is not internally inconsistent.

Fourthly, in section 8 of the Office Action, the Examiner objects to the use of a hyperlink on page 1, line 19. However, Applicants note that the full and proper citation to the EFI Specification is given in the DETAILED DESCRIPTION of the specification in paragraph [0036]. The citation used is entirely appropriate. The hyperlink being objected to by the Examiner was provided in the background section of the Application as an added benefit to simply direct the reader as to where **electronic copies** of publicly available EFI Specifications may be found. However, in response to the Examiner's concerns, a hardcopy of the cited EFI Specification is being submitted herewith in an Information Disclosure Statement.

In summary, Applicants do not believe the claims are indefinite. After reviewing the specification, Applicants note that the specification expressly defines all terms and phrases used in the claims in a clear and definite manner. The language used in the claims is consistent with the language used in the Specification. Evidence of this can be found in the fact that the Examiner quoted several of these definitions in the Office Action. Applicants' representative has reread the specification and finds it to be clear, complete, and fully enabling. FIGs. 4A and 4B clearly illustrate operation of the disclosed method, FIG. 3 clearly illustrates the invention from an architectural perspective, and FIG. 2 illustrates the concept of the invention. Great care was taken during drafting this specification to illustrates the invention at the concept level (FIG. 2), the architectural level (FIG. 3), and the operational level (FIGs. 4A and 4B).

Furthermore, FIG. 1 has been amended to cure the inadvertent error in the drawing. FIG. 1 now corresponds to the text of the background section (paragraph [0006]) to illustrate how prior art techniques mask/ignore legacy type hardware IRQs

while operating in the native mode runtime and mask/ignore native type hardware IRQs while operating in the legacy mode runtime.

CONCLUSION

In view of the foregoing remarks, Applicants believe the applicable rejections have been overcome and all claims remaining in the application are presently in condition for allowance. Accordingly, favorable consideration and a Notice of Allowance are earnestly solicited. The Examiner is invited to telephone the undersigned representative at (206) 292-8600 if the Examiner believes that an interview might be useful for any reason.

CHARGE DEPOSIT ACCOUNT

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a). Any fees required therefore are hereby authorized to be charged to Deposit Account No. 02-2666. Please credit any overpayment to the same deposit account.

Respectfully submitted,

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Date: April 3, 2006

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